REMARKS

These remarks are in response to the Office Action mailed on April 9, 2003. The Office Action rejected claims 52-70 under 35 U.S.C. 112, second paragraph, and rejected claims 29-35, 39, 40, 45, 46, 51, 53-57, 59 and 63 under 35 U.S.C. 102(b) as being anticipated by either Yamada *et al.* (U.S. patent number 5,068,827) or by Schrenk (U.S. patent number 4,279,024). The Office Action also objected to a number of claims.

Rejections under 35 U.S.C. 112, second paragraph

The Office Action rejected claims 52 and 53-70 due to some unusual features in the structure of claims 52 and 53. It appears that, in the course of preparing the application, the middle portion of claim 53 managed to end up between claims 52 and 53. The Applicants thank the Examiner for bringing this to their attention. Claims 52 and 53 have been amended to return the stray portion of claim 53 to its proper location, thereby removing the U.S.C. 112, second paragraph, rejections.

Rejections under 35 U.S.C. 102(b)

The Office Action rejected claims 29-35, 39, 40, 45, 46, and 51 under 35 U.S.C. 102(b) as being anticipated by Yamada *et al.* (U.S. patent number 5,068,827). Claim 29 is an independent claim upon which claims 30-35, 39, 40, 45, 46, and 51 depend. Claim 29 states:

> A method of operating of a non-volatile memory, comprising:
> applying a set of voltages to a storage unit of the non-volatile memory during an interval;
> determining the conduction characteristics of the storage unit in response to the set of voltages, wherein the set of voltages includes an episodic stimulus component.

The Office Action is correct that the Yamada *et al.* does describe "applying a set of voltages ..."; however, it is respectfully submitted that the second element ("determining the conduction characteristics ...") is not found in the Yamada references, either at cited location or elsewhere in the patent, and that the rejection under U.S.C. 102(b) is not well founded.

More specifically, the Office Action refers to Yamada's figure 6C and the description at column 6, line 65, to column 7, line 1. Figures 6A-D of Yamada, as described from column 5, line 61, to column 7, line 6, all relate to the *programming* of a non-volatile

semiconductor memory---in fact, the whole of Yamada's teachings are directed to programming techniques, as is clear from the title as well as the body of the specification. Figure 6A is a control gate voltage applied to a memory cell and Figure 6B is the resultant electric field across the cell's tunnel oxide. In response to this field, a Fowler-Nordheim current across this oxide occurs, which is shown in Figure 6C: that is, what Figure 6C shows is the resultant programming current *into the floating gate* in response to the programming pulse applied at the cell's control gate. This is quite different from the last element of claim 29.

The final element of claim 29 is "determining the conduction characteristics of the storage unit"; that is, determining the current flowing *through* the storage unit in response to applied voltages. For a memory element (such as the floating gate memory cell of Yamada), the conduction characteristics are related to the data content of the cell and "determining the conduction characteristics" is a read process. Consequently, this is quite different the cited process from Yamada, which is a programming process, and where Figure 6C shows the resultant programming current *into the floating gate* to place charge on the floating gate and not the determination of the charge flowing *through* the cell. Therefore, it is respectfully submitted that the rejection of claim 29 and its dependent claims 30-35, 39, 40, 45, 46, and 51 under 35 U.S.C. 102(b) as being anticipated by Yamada *et al.* is not well founded and should be withdrawn.

The Office Action also rejected dependent claims 30-35, 39, 40, 45, 46, and 51. These claims all recite additional features or limitations, which it is believed, make these claims further allowable. However, as the Office Action does not supply any specifics as to why these claims are rejected, they will not be discussed further at this time in order to same space.

The Office Action rejected claims 53-57, 59 and 63 under 35 U.S.C. 102(b) as being anticipated Schrenk (U.S. patent number 4,279,024). As noted above with respect to its rejection under 35 U.S.C. 112, second paragraph, claim 53 was originally presented in a corrupted form.

Claim 53 has been corrected and has drivers for applying both a sense voltage condition and an episodic stimulus:

> A non-volatile memory, comprising:
> a memory storage unit;

a sense amplifier connected to the memory storage unit for determining the state of the memory storage unit in response to a set of read voltages; and

drivers connected to the memory storage unit for applying the set of read voltages to the memory storage unit, the set of read voltages comprising:

a sense voltage condition; and

an episodic stimulus voltage condition.

The underlined portion was lacking in the original presentation. This differs from the Schrenk patent, which teaches the use of only a standard sense voltage condition.

More specifically, the Office Action refers to Figure 2g and column 9, lines 5-18, of Schrenk. However, this shows and describes only a standard prior art read process where a control gate voltage intermediate to the two data states (of, here, a binary cell) is applied to the control gate. Schrenk neither teaches nor suggests "drivers connected to the memory storage unit for applying ... to the memory storage unit ... a sense voltage condition; *and* an episodic stimulus voltage condition", where the empahsis is added.

Therefore, it is respectfully submitted that the rejection of claim 53 and its dependent claims 54-57, 59 and 63 under 35 U.S.C. 102(b) as being anticipated Schrenk is not well founded and should be withdrawn. The dependent claims 54-57, 59 and 63 all recite additional features or limitations, which it is believed, make these claims further allowable. However, as the Office Action does not supply any specifics as to why these claims are rejected, they will not be discussed further at this time in order to same space.

For any of these reasons, rejected claims 29-35, 39, 40, 45, 46, and 51-70 are believed allowable. Reconsideration of these claims is therefore respectfully requested and an early indication of their allowability is earnestly solicited.

Respectfully submitted,

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APPENDIX

1. A method of reading the data content of a non-volatile memory storage unit, comprising:

applying a set of sense voltage waveforms to the terminals of the memory storage unit during a read interval;

measuring a parameter value related to the data content of the memory storage unit during the read interval, wherein the measured value for the parameter includes the contribution of a noise component;

applying an episodic stimulus to the memory storage unit during the read interval, wherein the level of stimulus affects the parameter value and whereby the contribution of the noise component is reduced.

2. The method of claim 1, wherein the parameter is a current.

3. The method of claim 1, wherein the parameter is a voltage.

4. The method of claim 1, wherein the parameter is a time.

5. The method of claim 1, wherein the parameter is a frequency.

6. The method of claim 1, wherein the memory storage unit is a floating gate transistor and the measuring a parameter value comprises applying a non-periodic voltage to a first control gate of the transistor, and wherein the parameter is measured between a first and a second source/drain region of the transistor.

7. The method of claim 6, wherein the episodic stimulus is a periodic voltage waveform.

8. The method of claim 7, wherein the floating gate transistor further includes a select gate and the episodic stimulus is applied to the select gate.

9. The method of claim 7, wherein the episodic stimulus is applied to the first control gate of the transistor.

10. The method of claim 7, wherein the episodic stimulus is applied to the substrate of the transistor.

11. The method of claim 10, wherein the floating gate transistor has dual floating gates, the first control gate being located over a first of the dual floating gates, and further comprises a second control gate over the second of the dual floating gates, wherein the select gate is situated between the two control gates.

12. The method of claim 7, wherein the periodic voltage has a sinusoidal wave form.

13. The method of claim 7, wherein the periodic voltage has a rectangular wave form.

14. The method of claim 7, wherein the periodic voltage has a trapezoidal wave form.

15. The method of claim 6, wherein the parameter is the current flowing in a channel region of the floating gate transistor.

16. The method of claim 6, wherein the parameter is a voltage required to established a predetermined current.

17. The method of claim 6, wherein the episodic stimulus is a single voltage pulse.

18. The method of claim 6, wherein the read interval comprises a first phase and a subsequent second phase, wherein the measuring a parameter is performed during

the second phase and the applying a set of sense voltage waveforms begins during the first phase.

19. The method of claim 18, wherein the episodic stimulus are multiple voltage pulses.

20. The method of claim 18, wherein the episodic stimulus is applied during the second phase.

21. The method of claim 18, wherein the episodic stimulus is applied during the first phase.

22. The method of claim 1, wherein the memory storage unit is a magnetic memory cell and the episodic stimulus is a magnetic field.

23. The method of claim 1, wherein the wherein the memory storage unit is a molecular transistor memory storage unit.

24. The method of claim 1, wherein the wherein the memory storage unit is a single electron transistor memory storage unit.

25. The method of claim 1, wherein the wherein the memory storage unit is a nano-transistor memory storage unit.

26. The method of claim 1, wherein said applying an episodic stimulus is invoked in response to an error control coding result.

27. The method of claim 1, wherein said read interval comprises a first portion and a subsequent second portion, and wherein said applying a set of sense voltage waveforms comprises:

applying a first set of sense voltage waveforms to the terminals of the memory storage unit during the first portion of the read interval; and

applying a second set of sense voltage waveforms to the terminals of the memory storage unit during the second portion of the read interval;

wherein said measuring the parameter value comprises:

measuring the parameter value related to the data content of the memory storage unit during the first portion of the read interval; and

measuring a parameter value related to the data content of the memory storage unit during the second portion of the read interval; and

wherein said applying an episodic stimulus is performed during the second portion of the read interval in response to said measuring the parameter value related to the data content of the memory storage unit during the first portion of the read interval.

28. The method of claim 27, wherein said applying an episodic stimulus is invoked in response to an error control coding result.

29. A method of operating of a non-volatile memory, comprising:

applying a set of voltages to a storage unit of the non-volatile memory during an interval;

determining the conduction characteristics of the storage unit in response to the set of voltages, wherein the set of voltages includes an episodic stimulus component.

30. The method of claim 29, wherein the determining the conduction characteristics comprises measuring a current.

31. The method of claim 29, wherein the determining the conduction characteristics comprises measuring a voltage.

32. The method of claim 29, wherein the determining the conduction characteristics comprises measuring a time.

33. The method of claim 29, wherein the determining the conduction characteristics comprises measuring a frequency.

34. The method of claim 29, wherein the memory storage unit is a floating gate transistor and the set of voltages further includes applying a non-periodic voltage to a first control gate of the transistor, wherein the determining the conduction characteristics includes measuring a parameter between a first and a second source/drain region of the transistor during a read interval.

35. The method of claim 34, wherein the episodic stimulus is applied to the control gate of the transistor.

36. The method of claim 34, wherein the episodic stimulus is applied to the substrate of the transistor.

37. The method of claim 34, wherein the floating gate transistor further comprises a select gate and the episodic stimulus is applied to the select gate.

38. The method of claim 37, wherein the floating gate transistor has dual floating gates, the first control gate being located over the first of the dual floating gates, and further comprises a second control gate over the second of the dual floating gates, wherein the select gate is situated between the two control gates.

39. The method of claim 34, wherein the parameter is the current flowing in a channel region of the floating gate transistor.

40. The method of claim 34, wherein the parameter is a voltage required to established a predetermined current.

41. The method of claim 34, wherein the read interval comprises a first phase and a subsequent second phase, wherein the measuring a parameter is performed during the second phase and applying a set of sense voltage waveforms beginning during the first phase.

42. The method of claim 41, wherein the episodic stimulus is applied the second phase.

43. The method of claim 41, wherein the episodic stimulus is applied the first phase.

44. The method of claim 29, wherein the episodic stimulus is a voltage having a sinusoidal waveform.

45. The method of claim 29, wherein the episodic stimulus is a voltage having a rectangular wave form.

46. The method of claim 29, wherein the episodic stimulus is a voltage having a trapezoidal wave form.

47. The method of claim 29, wherein the memory storage unit is a magnetic memory cell and the episodic stimulus is a magnetic field.

48. The method of claim 29, wherein the wherein the memory storage unit is a molecular transistor memory storage unit.

49. The method of claim 29, wherein the wherein the memory storage unit is a single electron transistor memory storage unit.

50. The method of claim 29, wherein the wherein the memory storage unit is a nano-transistor memory storage unit.

51. The method of claim 29, wherein said determining the conduction characteristics of the storage unit comprises:

determining a first time the conduction characteristics of the storage unit in response to the set of voltages; and

subsequently determining a second time the conduction characteristics of the storage unit in response to the set of voltages, wherein the episodic stimulus component is applied only during said determining a second time.

52.(Amended) The method of claim 51, wherein said subsequently determining a second time the conduction characteristics of the storage unit is in response to error control coding result.

53.(Amended) A non-volatile memory, comprising:

a memory storage unit;

a sense amplifier connected to the memory storage unit for determining the state of the memory storage unit in response to a set of read voltages; and

drivers connected to the memory storage unit for applying the set of read voltages to the memory storage unit, the set of read voltages comprising:

a sense voltage condition; and

an episodic stimulus voltage condition.

54. The memory of claim 53, wherein the sense amplifier operates by sensing a current.

55. The memory of claim 53, wherein the sense amplifier operates by sensing a voltage.

56. The memory of claim 53, wherein the memory storage unit is a floating gate transistor and the sense voltage condition includes applying a voltage to a first control gate of the transistor, wherein the sense amplifier measures a parameter between a first and a second source/drain region of the transistor.

57. The memory of claim 56, wherein the episodic stimulus voltage condition is applied to a control gate of the transistor.

58. The memory of claim 56, wherein the episodic stimulus voltage condition is applied to the substrate of the transistor.

59. The memory of claim 56, wherein the floating gate transistor further comprises a select gate and the episodic stimulus voltage condition is applied to the select gate.

60. The memory of claim 59, wherein the floating gate transistor has dual floating gates, the first control gate being located over a first of the dual floating gates, and further comprises a second control gate over the second of the dual floating gates, wherein the select gate is situated between the two control gates.

61. The memory of claim 56, wherein the parameter is the current flowing in a channel region of the floating gate transistor.

62. The memory of claim 56, wherein the parameter is a voltage required to establish a predetermined current.

63. The memory of claim 53, wherein the episodic stimulus voltage condition is a periodic voltage having a rectangular wave form.

64. The memory of claim 53, wherein the episodic stimulus voltage condition is a periodic voltage having a trapezoidal wave form.

65. The memory of claim 53, further comprising:

an error control code section coupled to the sense amplifier and to the drivers, wherein said drivers apply the episodic stimulus voltage condition in response to a control signal from the error control code section.

66. The method of claim 53, wherein the memory storage unit is a magnetic memory cell and the episodic stimulus is a magnetic field.

67. The method of claim 53, wherein the wherein the memory storage unit is a molecular transistor memory storage unit.

68. The method of claim 53, wherein the wherein the memory storage unit is a single electron transistor memory storage unit.

69. The method of claim 53, wherein the wherein the memory storage unit is a nano-transistor memory storage unit.

70. The memory of claim 53, wherein the non-volatile memory comprises an array of storage units of which said memory storage unit is a member, further comprising:

a booster line connected between one of said drivers and a portion of the array including said memory storage unit whereby said episodic stimulus voltage condition is applied.